A Reconfigurable 10MS/s to 100MS/s, 0.5V to 1.2V, 0.98mm$^2$, 10b Low-Power 0.13um CMOS Pipeline ADC

ABSTRACT

This work describes a reconfigurable 10MS/s to 100MS/s, 0.5V to 1.2V, 0.98mm$^2$, 10b low-power 0.13um CMOS two-step pipeline ADC. The SHA employs gate-bootstrapped sampling switches and a two-stage amplifier based on a low-threshold NMOS differential input stage to obtain 10b accuracy even at a 0.5V supply. A signal-isolated all directionally symmetric layout reduces the MDAC capacitor mismatch while the flash ADCs employ a switched-bias power-reduction technique to reduce the power consumption of comparators. The CMOS on-chip I/V references operate at a supply ranging from 0.5V to 1.2V with optional off-chip voltage references. The prototype ADC in a 0.13um CMOS process demonstrates the measured DNL and INL within 0.35LSB and 0.49LSB, respectively. The ADC with an active die area of 0.98mm$^2$ shows the maximum SNDR and SFDR of 52dB and 65dB, respectively, and a power consumption of 22.4mW at a typical condition, 0.8V and 70MS/s.

I. INTRODUCTION

As recently developed very large-scale integration (VLSI) technologies enable a number of transistors to be integrated on a single chip, the system-on-a-chip (SoC) trend is expected to be a desirable future solution for a variety of high-performance system applications. The SoC reduces the
total manufacturing cost, improves the system performance, and minimizes the chip size. However, advanced deep sub-micron process technologies primarily for high-density high-speed digital circuits have continuously demanded low power supplies below 1V. The reduced power supplies increase the on-resistance of analog switches and decrease the signal bandwidth and swing margin of essential analog circuits, especially, for the mixed-signal SoC. The typical mixed-signal SoC interface needs a wide specification of analog signal processing circuits such as analog-to-digital converters (ADCs) and employs considerably different levels of power supply depending on applications even with the same process technology. For example, the ADCs for high-definition portable video applications and high-quality communication systems such as wireless local area network (WLAN) based on IEEE 802.11 require, at least, a resolution of 10b, a sampling rate of several tens of MS/s, a small chip area, and a low-power consumption while operating at a wide range of power supply.

Of numerous conventional ADC architectures, the pipeline architecture has been widely employed to meet the required flexible specifications. In the multi-bit-per-stage pipeline ADCs, the more bits are decided in the front-end stage, the less noise and device mismatch errors from the back-end stages are input-referred. The power consumption and chip area of the ADCs can be also reduced since the fewer number of inter-stage amplifiers are used. However, the increased closed-loop gain and the large load capacitance of inter-stage amplifiers tend to limit the maximum conversion speed of the ADCs. The comparator offsets may also affect the accuracy in the sub-ranging flash ADCs since more bits need to be decided in each pipeline stage. On the other hand, the single-bit-per-stage or the multi-bit-per-stage pipeline ADCs to decide fewer bits in each stage can process analog signals at a higher speed than the multi-bit-per-stage ADCs to decide more bits in each stage due to the reduced load capacitance and closed-loop gain of inter-stage amplifiers. However, since the single-bit-per-stage architecture requires more pipeline stages, more power consumption, and larger chip area, the increased input-referred noise and device mismatch from the back-end pipeline stages can degrade the ADC static and dynamic performances considerably.
The recently reported 10b CMOS pipeline ADCs with a sampling rate exceeding tens of MS/s and the proposed 10b ADC are compared in Fig. 1 [1]-[21]. As shown in Fig. 1, most of the ADCs are based on the multi-bit-per-stage pipeline architecture with more than three stages. The proposed ADC employs a two-step pipeline architecture to optimize its power and chip area, considering the above-mentioned advantages and disadvantages. Above all, as far as the authors know, the proposed ADC is the unique one operating at a 0.5V supply voltage when compared with the recently reported ADCs showing the similar specifications. The prototype ADC demonstrates nearly the world-highest power efficiency of 0.3mW/MHz at a power supply ranging from 0.5V to 0.8V.

Fig. 1. Power and sampling speed of recently reported 10b CMOS ADCs.

In this work, the proposed reconfigurable 10b ADC employs (1) a two-step pipeline architecture to optimize conversion speed, power consumption, and chip area, (2) MOS transistors with a low-threshold voltage of 0.35V in gate-bootstrapped input sampling switches and differential input stages of the sample-and-hold amplifier (SHA) based on a two-stage amplifier to obtain high static and dynamic performances at 0.5V supply level, (3) a signal-isolated all directionally symmetric layout technique to minimize the capacitor and device mismatch in the multiplying D/A converter (MDAC), (4) a switched-bias power-reduction technique to reduce the power consumption of comparators in the 5b and 6b sub-ranging flash ADCs, and (5) the on-chip full CMOS current and voltage (I/V)
references to operate at a supply voltage ranging from 0.5V to 1.2V with optional off-chip voltage references. The proposed ADC architecture is discussed in Section II. Section III briefly describes circuit implementation and layout techniques. The measured results of the prototype ADC are summarized in Section IV.

II. PROPOSED ADC ARCHITECTURE

The proposed 10b CMOS ADC as illustrated in Fig. 2 consists of an input SHA, a 5b MDAC, 5b and 6b flash ADCs, on-chip I/V references, digital circuits such as digital correction logic (DCL), decimator, and clock generator. The non-overlapping Q1 and Q2 clock phases are internally generated.

![Diagram of proposed ADC architecture](image)

Fig. 2. Proposed reconfigurable 10b ADC.

Nonlinear errors such as offsets and clock feed-through errors between pipeline stages are digitally corrected in the DCL by overlapping 1b from 11b raw codes to obtain 10b outputs. The on-chip decimator samples the 10b outputs of the prototype ADC at a full, a half, or a quarter conversion speed accurately to evaluate the ADC dynamic performance by minimizing the glitch and transient noise coming from the performance evaluation board.
III. CIRCUIT IMPLEMENTATION

1. Proposed SHA with low-threshold gate-bootstrapped sampling switches

The SHA operation at a low supply voltage is commonly limited by high on-resistance of input sampling switches due to the decreased overdrive voltage ($V_{gs}-V_{th}$). The wideband low-distortion SHA requires input sampling switches with a low parasitic capacitance as well as a low and constant on-resistance. Conventional CMOS switches hardly meet the requirements of a resolution of 10b and a conversion speed of tens of MS/s at a low supply voltage below 1V due to the signal-dependent resistance variations and low gate-driving voltages of sampling switches. The proposed input SHA as illustrated in Fig. 3 employs the gate-bootstrapping technique to minimize the nonlinear distortion of sampled inputs due to the on-resistance variations of switches by keeping the gate-source voltage of input sampling switches constant [2]. Moreover, the input sampling switches adopt NMOS devices with a low-threshold voltage to implement a low parasitic capacitance and to properly handle the Nyquist input frequency even at a 0.5V supply voltage. The SHA sampling capacitance is 1.2pF considering the required 10b accuracy and kT/C noise at a 0.8V_p-p full-scale input.

Fig. 3. SHA with gate-bootstrapped sampling switches.
2. Low-voltage amplifier for the SHA and MDAC

The proposed ADC requires low-voltage amplifiers as well as input sampling switches to operate reliably even at a 0.5V supply voltage. The SHA and MDAC employ a two-stage amplifier to achieve the sufficient DC gain and output swing margin for 10b accuracy as shown in Fig. 3. The folded-cascode architecture is employed in the first stage amplifier primarily to achieve a high DC gain while the unfolded-cascode architecture is needed in the second stage amplifier to obtain a high output swing margin at a low supply voltage. Particularly, in the input stage of amplifiers, NMOS transistors with a low-threshold voltage are used simultaneously to achieve a low parasitic capacitance, a high signal swing margin, and a high trans-conductance for the required bandwidth and sampling rate at a resolution of 10b and a 0.5V supply.

3. All directionally symmetric highly linear MDAC capacitors

The capacitor mismatch in the MDAC is very critical to the ADC static and dynamic performances. The capacitor mismatch is caused by random errors and systematic errors. Random errors are caused by process variations such as inaccurate etching and oxide thickness variations while systematic errors are caused by different parasitic capacitances between capacitors and adjacent signal lines. Many inventive calibration techniques have overcome the device or capacitor mismatch problems of the ADCs for a high resolution exceeding 10b. However, most of calibration techniques with complicated algorithms tend to increase chip area, power consumption, and engineering cost. As deep sub-micron technologies have been continuously developed, random errors have been decreased as well. Systematic errors can be also reduced only by layout techniques without additional calibration circuits [22], [23]. The MDAC capacitor layout proposed in this work for high matching is shown in Fig. 4.
Fig. 4. Signal-isolated all directionally symmetric high-matching capacitor layout.

The proposed ADC uses only 4 metal lines for low cost in a 1P6M CMOS technology. The proposed MDAC capacitors in Fig. 4 are based on a metal-insulator-metal (MIM) structure. All the symmetric unit capacitors are enclosed by all other metals except the metals for routing the top and bottom plates of capacitors. Each unit capacitor has the identical environment to all directions and achieves high capacitor matching accuracy. In the previously published layout technique [23], both unit capacitors and bottom-plate signal lines are isolated with all the employed metal lines. This method makes capacitors to be surrounded physically in the same environment. However, some signal lines passing through neighboring capacitors and unit capacitors may have functionally different parasitic capacitances each other.

On the other hand, the proposed signal-isolated all directionally symmetric layout technique in Fig. 4 integrates additional metal lines between signal lines connecting the bottom plates of capacitors, which minimizes capacitor mismatch physically and functionally by isolating each unit capacitor from all the neighboring signal lines. The conventional dummy capacitors surrounding the whole unit-capacitor zone further reduce mismatch between unit capacitors caused by process variations. The proposed 5b MDAC employs a merged-capacitor switching technique to reduce the number of required unit capacitors from 32 to 16 for low power, high density, and low noise coupling [24]. The unit capacitor size of the MDAC is designed to be 100fF, considering the kT/C noise and the desired 10b capacitor matching.
4. Switched-bias power-reduction technique for two flash ADCs

The proposed ADC needs two sub-ranging flash ADCs, FLASH1 and FLASH2, generating coarse 5b and fine 6b digital codes, respectively. The comparators in the FLASH1 and FLASH2 are composed of a two-stage pre-amplifier with an open-loop offset sampling network and a latch for the required sampling speed and accuracy at a 0.5V to 1.2V supply range with a 0.8V differential reference voltage, as shown in Fig. 5.

![Fig. 5. Pre-amplifier in the FLASH1 and FLASH2 comparators.](image)

The flash ADCs employ a switched-bias power-reduction technique to minimize the power consumption of pre-amplifiers [6]. During the input and offset sampling mode, the second-stage pre-amplifier consumes unnecessary power. With the controlled bias voltage of BIAS2 in Fig. 5, the second-stage pre-amplifier bias current is completely turned off. During the next amplifying mode, the pre-amplifier bias current is completely resumed. As a result, the proposed flash ADCs consume less power by 20% than those without using the power-reduction technique.

5. Full CMOS on-chip current and voltage references

The ADC proposed in this work implements full CMOS current and voltage references on a chip properly to operate at a low supply voltage ranging from 0.5V to 1.2V with optional off-chip voltage
references, as shown in Fig. 6. The typical band-gap voltage reference is difficult to operate at sub-1V supplies due to the band-gap voltage limitation of 1.25V [25].

The external reference control code (EXTRF) in Fig. 6 decides to use either on-chip or off-chip voltage references. With the EXTRF high, two reference output nodes are in a high impedance state, which makes it possible to use off-chip references. It is noted that the ADC has a power-off (POFF) mode for low-power potable applications. With the POFF set to high, the ADC power consumption is reduced to 3uW. With the POFF set to low, the ADC returns to the normal active mode approximately within 1us. The IREF block in Fig. 6 generates on-chip reference currents insensitive to power-supply and temperature variations. The current mismatch within ±30% can be calibrated in the digital domain by the 3b IVCN digital code [26].

Recently developed high-resolution CMOS ADCs based on a switched-capacitor technique have supplied the required reference voltages to internal circuits through MOS switches. These reference voltages tend to contain high transient glitches and high-frequency switching noise due to repeated charging and discharging operations. Simple on-chip RC filters integrated with the references considerably reduce the high-frequency switching noise at the reference voltage outputs and minimize the settling time even at a maximum sampling rate, 100MS/s, without large conventional off-chip
decoupling capacitors of several uF level. As demonstrated in the simulation results of Fig. 7, the REFTOP and REFBOT nodes with on-chip RC filters alone (Case I) and with both of on-chip RC filters and 0.1uF off-chip decoupling capacitors (Case II) show almost the same signal settling behavior and time.

![Simulated on-chip top and bottom reference voltages.](image)

Fig. 7. Simulated on-chip top and bottom reference voltages.

**IV. PROTOTYPE ADC MEASUREMENTS**

The prototype ADC is fabricated in a 0.13um n-well 1P6M CMOS process. The proposed ADC has a limited number of external pins such as inputs, outputs, and power supplies primarily for the use as one of core blocks of large integrated systems. The chip photograph of the prototype ADC is shown in Fig. 8, where the blocks encircled by bold and dotted lines indicate on-chip PMOS and NMOS decoupling capacitors, respectively. The total on-chip MOS capacitors of about 265pF for two reference voltages and two power supplies effectively suppress the EMI problems and the random noise coupling from different functional circuit blocks.
The prototype ADC occupies an active die area of 0.98mm$^2$ (=1.20mm $\times$ 0.82mm) and dissipates 22.4mW at a typical operating condition, 0.8V and 70MS/s. As illustrated in Fig. 9, the measured differential non-linearity (DNL) and integral non-linearity (INL) are within 0.35LSB and 0.49LSB, respectively.

A typical signal spectrum of the prototype ADC measured with 70MS/s at a 1MHz input and a 0.8V supply voltage is plotted in Fig. 10.
Fig. 10. Signal spectrum measured with a 1MHz input signal at 70MS/s.

The signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) in Fig. 11(a) are measured with different sampling frequencies up to 70MS/s at a 1MHz input and a 0.8V supply. The SNDR and SFDR are maintained over 56dB and 70dB, respectively up to 60MS/s. With a maximum sampling frequency of 70MS/s at 0.8V, the measured SNDR and SFDR are 52dB and 65dB, respectively. The SNDR and SFDR in Fig. 11(b) are measured with increasing input frequencies at a maximum sampling frequency of 70MS/s and a 0.8V supply voltage. As shown in Fig. 11(b), the prototype ADC maintains the constant SNDR and SFDR with input frequencies increased to the Nyquist frequency.
Fig. 11. Measured SFDR and SNDR versus (a) fs and (b) fin.

The maximum sampling frequency and the corresponding power consumption of the proposed ADC are measured at operating voltages from 0.5V to 1.8V, as illustrated in Fig. 12. The prototype ADC demonstrates nearly the world-best power efficiency of 0.3mW/MHz at 0.5V to 0.8V supply voltages. The measured performance of the prototype ADC is summarized in Table I. The proposed ADC is compared with the recently reported 10b pipeline CMOS ADCs operating at sub-1.2V supplies in Table II. The proposed prototype ADC is almost the unique version operating at a 0.5V supply voltage with a 10b resolution and tens of MS/s, demonstrating very high power efficiency and linearity.

Fig. 12. Measured power dissipation versus supply and sampling frequency.
Table I. Performance summary of the prototype ADC.

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<table>
<thead>
<tr>
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<th></th>
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</thead>
<tbody>
<tr>
<td><strong>Resolution</strong></td>
<td>10bits</td>
<td></td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td>0.5V ~ 1.2V (Nominal 0.8V)</td>
<td></td>
</tr>
<tr>
<td><strong>Conversion Rate</strong></td>
<td>10MS/s ~ 100MS/s (Nominal 70MS/s)</td>
<td></td>
</tr>
<tr>
<td><strong>Process</strong></td>
<td>Samsung 0.13um CMOS (with MIM Capacitor)</td>
<td></td>
</tr>
<tr>
<td><strong>Input Range / On-Chip Reference</strong></td>
<td>0.8Vpp (Fixed, Off-chip ref. optional)</td>
<td></td>
</tr>
<tr>
<td>SNDR (@ 0.8V, 60MS/s)</td>
<td>56.0dB (@ fin= 1MHz)</td>
<td></td>
</tr>
<tr>
<td>SNDR (@ 0.8V, 70MS/s)</td>
<td>51.7dB (@ fin= 1MHz)</td>
<td></td>
</tr>
<tr>
<td>SFDR (@ 0.8V, 60MS/s)</td>
<td>69.6dB (@ fin= 1MHz)</td>
<td></td>
</tr>
<tr>
<td>SFDR (@ 0.8V, 70MS/s)</td>
<td>65.2dB (@ fin= 1MHz)</td>
<td></td>
</tr>
<tr>
<td><strong>DNL / INL</strong></td>
<td>0.35LSB / 0.49LSB</td>
<td></td>
</tr>
<tr>
<td><strong>ADC Power</strong></td>
<td>3.0mW (@ 0.5V / 10MS/s)</td>
<td>22.4mW (@ 0.8V / 70MS/s)</td>
</tr>
<tr>
<td><strong>Active Die Area</strong></td>
<td>0.98mm² (= 1.20mm × 0.82mm)</td>
<td></td>
</tr>
</tbody>
</table>

Table II. Recently reported 10b CMOS ADCs operating below a 1.2V supply.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Speed. (MS/s)</th>
<th>Supply (V)</th>
<th>Power (mW)</th>
<th>Area (mm²)</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>10 ~ 100</td>
<td>0.5 ~ 1.2</td>
<td>3.0 ~ 45.6</td>
<td>0.98</td>
<td>0.35</td>
<td>0.49</td>
</tr>
<tr>
<td>ESSCIRC 06 [5]</td>
<td>20</td>
<td>1.2</td>
<td>5.0</td>
<td>0.26</td>
<td>0.80</td>
<td>1.70</td>
</tr>
<tr>
<td>CICC 06 [6]</td>
<td>25</td>
<td>1.2</td>
<td>4.8</td>
<td>0.80</td>
<td>0.42</td>
<td>0.91</td>
</tr>
<tr>
<td>ISSCC 06 [10]</td>
<td>50</td>
<td>1.2</td>
<td>15.0</td>
<td>0.20</td>
<td>0.17</td>
<td>0.16</td>
</tr>
<tr>
<td>CICC 06 [13]</td>
<td>80</td>
<td>1.2</td>
<td>47.0</td>
<td>1.92</td>
<td>0.93</td>
<td>2.21</td>
</tr>
<tr>
<td>VLSI 06 [17]</td>
<td>100</td>
<td>1.0</td>
<td>30.0</td>
<td>4.03</td>
<td>0.50</td>
<td>0.80</td>
</tr>
<tr>
<td>CICC 05 [18]</td>
<td>100</td>
<td>1.0</td>
<td>40.0</td>
<td>0.52</td>
<td>0.38</td>
<td>0.96</td>
</tr>
<tr>
<td>ESSCIRC 05 [21]</td>
<td>200</td>
<td>1.2</td>
<td>55.0</td>
<td>2.52</td>
<td>0.66</td>
<td>1.00</td>
</tr>
</tbody>
</table>
V. CONCLUSION

This work proposes a reconfigurable 10MS/s to 100MS/s, 0.5V to 1.2V, 0.98mm$^2$, 10b low-power 0.13um CMOS two-step pipeline ADC for WLAN and high-quality image signal processing applications. The ADC is based on the following circuit design techniques. First, the proposed 10b ADC adopts a two-step pipeline architecture to optimize chip area and power consumption at a sampling rate of 10MS/s to 100MS/s. Second, the SHA with a high signal-swing range employs gate-bootstrapped MOS sampling switches and a two-stage amplifier based on folded- and unfolded-cascode architectures with a low-threshold NMOS differential input stage to achieve high static and dynamic performances even at 0.5V supply level. Third, the MDAC implements a signal-isolated all directionally symmetric layout to minimize the capacitor mismatch. Fourth, the sub-ranging flash ADCs are based on a switched-bias power-reduction technique to reduce the power consumption of comparators. Finally, the full CMOS on-chip I/V references operate at a supply voltage ranging from 0.5V to 1.2V with optional off-chip voltage references.

The prototype ADC implemented in a 0.13um 1P6M CMOS technology demonstrates the measured DNL and INL within 0.35LSB and 0.49LSB, respectively. The prototype ADC shows the maximum SNDR and SFDR of 52dB and 65dB, respectively, a power consumption of 22.4mW at 0.8V and 70MS/s, and an active die area of 0.98mm$^2$. 
REFERENCES


